CLAIMS

1. (Original) A method for performing circuit analysis on a circuit design, comprising:

determining instantiation paths for one or more design blocks of the circuit design;

recursively accumulating select information for each of the design blocks; and

applying instantiation characteristics to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design.

2. (Original) The method of claim 1, the select information comprising one or more of FET capacitance, FET width and wire capacitance.

3. (Original) The method of claim 1, the instantiation characteristics comprising one or more of switching frequencies and scaling factors.

4. (Currently Amended) The method of claim 1, the step of recursively accumulating comprising recursively accumulating selected information for one or more highest level signal name (HLSN) signal nets within the design blocks.

5. (Currently Amended) The method of claim 4, further comprising selecting the one or more highest level signal names (HLSNs) through a user interface.

6. (Original) The method of claim 1, further comprising selecting the one or more blocks through a user interface.

7. (Original) The method of claim 1, further comprising reading instantiation hierarchy from the circuit design to determine the instantiation paths.

8. (Original) The method of claim 1, further comprising reading instantiation characteristics from the circuit design.

9. (Original) The method of claim 1, further comprising generating results based upon applied instantiation characteristics.

10. (Original) A system for performing circuit analysis on a circuit design, comprising:

a user interface for selecting one or more design blocks of the circuit design;

an analysis tool operable to determine instantiation paths for the design blocks, accumulate select information for each instance of each of the design blocks, and apply instantiation characteristics of each instance to the accumulated information; and

memory for storing the instantiation paths, the accumulated information, and results based upon the applied characteristics.

11. (Original) The system of claim 10, the select information comprising one or more of FET capacitance, FET width and wire capacitance.

12. (Original) The system of claim 10, the instantiation characteristics comprising one or more of switching frequencies and scaling factors.

13. (Currently Amended) The system of claim 10, the analysis tool operable to recursively accumulate the select information for one or more highest level signal name (HLSN) signal nets within the design blocks.

14. (Original) The system of claim 10, wherein the analysis tool is operable to read an instantiation hierarchy of the circuit design to determine the instantiation paths

15. (Original) The system of claim 14, wherein the analysis tool is operable to read the instantiation characteristics from the circuit design.

16. (Original) A system for performing circuit analysis on a circuit design, comprising:

means for determining instantiation paths for one or more design blocks of the circuit design;

means for recursively accumulating select information for each of the design blocks; and

means for applying instantiation characteristics to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design.

17. (Original) The system of claim 16, the select information comprising one or more of FET capacitance, FET width and wire capacitance.

18. (Original) The system of claim 16, the instantiation characteristics comprising one or more of switching frequencies and scaling factors.

19. (Currently Amended) The system of claim 16, the means for recursively accumulating comprising means for recursively accumulating select information of one or more highest level signal name (HLSN) signal nets of the design blocks.

20. (Original) The system of claim 16, further comprising means for reading instantiation hierarchy from the circuit design to determine the instantiation paths.

21. (Original) The system of claim 16, further comprising means for reading instantiation characteristics from the circuit design.

22. (Original) The system of claim 16, further comprising means for generating results based upon applied instantiation characteristics.

23. (Original) A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for performing circuit analysis on a circuit design, comprising:

instructions for determining instantiation paths for one or more design blocks of the circuit design;

instructions for recursively accumulating select information for each of the design blocks; and

instructions for applying instantiation characteristics to the accumulated information for each instance of the design blocks based upon instantiation hierarchy of the instance within the circuit design.

24. (Original) The software product of claim 23, the select information comprising one or more of FET capacitance, FET width and wire capacitance.

25. (Original) The software product of claim 23, the instantiation characteristics comprising one or more of switching frequencies and scaling factors.

26. (Currently Amended) The software product of claim 23, wherein the instructions for recursively accumulating comprise instructions for recursively accumulating the select information for one or more highest level signal name (HLSN) signal nets within the design blocks.

27. (Original) The software product of claim 23, further comprising instructions for reading instantiation hierarchy from the circuit design to determine the instantiation paths.

28. (Original) The software product of claim 23, further comprising instructions for reading instantiation characteristics from the circuit design.

29. (Original) The software product of claim 23, further comprising instructions for generating results based upon applied instantiation characteristics.